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DESIGN AND SIMULATION OF HIGH PERFORMANCE SENSE AMPLIFIER FOR LOW POWER SRAM

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ABSTRACT

A high performance sense amplifier circuit is used to construct SRAM. The research work aims at using multiple techniques for power optimization of SRAM cell or complete SRAM chip. Through this paper, we propose a systematic approach for enhancing the performance of SRAM cell by using sense amplifier circuit. The transistor stage number of the proposed design from VDD to GND is reduced for fast low voltage operation. Thus the proposed sense amplifier which is implemented in 180nm CMOS process can work at 100MHz with voltage as low as 1.2V. The improvement of sensing delay is reduced by 16% for various output loading. As the sense amplifier works at 1.2V, the simulations show that this design has 59% power improvement over the conventional sense amplifier.

KEYWORDS: SRAM Cell, Power Dissipation, Sense Amplifier

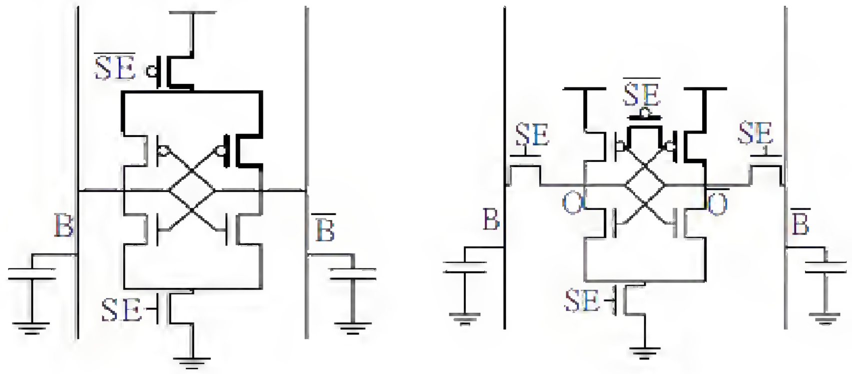
INTRODUCTION

The Static Random Access Memory (SRAM) is a very popular application of VLSI. Generally speaking, a SRAM array includes the following parts: input buffer, row decoder, column decoder, sense amplifier, memory cell and output buffer [1]. The reading access time of SRAM is an important performance parameter.

Furthermore, the sense amplifier usually lies in the speed bottleneck of SRAM access time. Sensing and amplifying the data signal which transmits through memory cell to bit line are the most important function for a sense amplifier. However, to sense the data correct and fast becomes more and more difficult when the working voltage scales down with the gate oxide thickness. Because the bit lines are always loaded by a large number of memory cells, the loading of bit lines are usually pretty large. Thus, the signal swing distributed on bit line will be an inverse ratio to the loading of bit line (about 50mV~200mV). So the sensing delay becomes one of the bottlenecks of memory reading access time. With the decrease of working voltage, the input signal swing of sense amplifier is becoming smaller. This result leads to a challenge for sense amplifier to work at a lower working voltage.

In Figure 1(a), it is a full-complementary positive-feedback sense amplifier [2], [3]. This circuit is a very common and simple sense amplifier in DRAM applications. It can sense and amplify the signal on bit line directly. So that, when DRAM cell is charged or discharged by the voltage difference between precharge voltage and cell voltage, this sense amplifier can write the original data value back to DRAM cell which has been selected. But in SRAM applications, this design becomes less useful because SRAM cells don't need to write back data when sensing data. And the loading of bit lines is so large that it will cause longer sensing delay and larger power dissipation. Thus, this design is not often used in SRAM applications. However, another SA design which is shown in Figure 1(b) [4], [5] has a better performance than previous SA in Figure 1(a). The SA has two decouple transistors between their bit lines and output nodes. The two decouple transistors isolate the loading of output nodes because the bit line loading is decoupled from output nodes and a

lot of improvement has been made in the sensing delay. However, there still exists a current flow, which is caused from the voltage difference between bit lines to output nodes, from bit lines to output nodes when the sensing signal SE is at logic 1. This current flow makes additional and unexpected power dissipation when sense amplifier senses data signal from bit line. So if we want to save sensing power, we have better to isolate the output node from input node (bit line). The following SA design is one kind of SA which input nodes and output nodes are isolated.



(a) (b)

Figure 1: Conventional SA (a) Full-Complementary Positive-Feedback SA Circuit (b) Positive-Feedback SA Circuit with Decouple Device

Current Latched Sense Amplifier

The Current Latched Sense Amplifier (CLSA) [6], [7] is shown in Figure 2. The bit line signal difference affects on the gate voltage of transistors MN1 and MN2, and the drains of transistors MP1, MN5, MP2 and MN4 are output nodes.

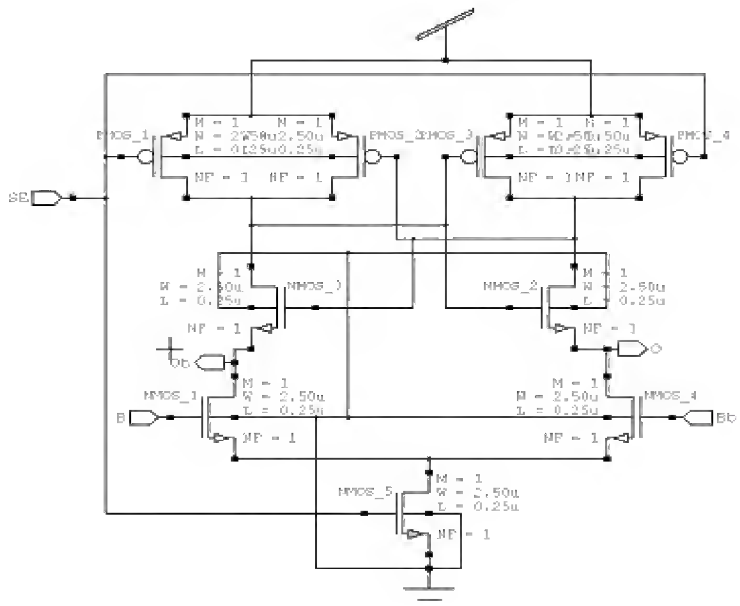


Figure 2: Current Latched Sense Amplifier

There is no current flow from bit lines to output nodes. When sensing signal SE is at logic 0 (GND), the output node is isolated to GND, and the precharge transistors MP3, MP4 charge output nodes to VDD. Because the output nodes O and Ob are precharged to VDD, the transistors MP1, MP2 are at cut-off region and MN4, MN5 are at saturation region. When the sensing signal SE changes to logic 1 (VDD), MN3 is turned on and the node S is pulled down to GND level.

Under this condition, MN1 and MN2 are working as a common source differential amplifier. The voltage difference between B and B is transferred to the output nodes O and ℵ by the common source differential amplifier. After a small voltage difference between O and Ob is generated, the cross-coupled amplifier which is constructed by MN4, MN5, MP1 and MP2 will finally amplify the voltage difference between O and Ob to a full swing voltage level. Therefore, we can sense and amplify the bit line signal without any current drifting from bit line to output node. This result shows that the b it line voltages will not be amplified, so the sensing and precharging power dissipation will be reduced. However, the CLSA has four transistors cascaded from VDD to GND. This is a major disadvantage of CLSA to work at low working voltage (under 1.2v). When CLSA is working at low voltage, the differential current may be too small to be used for fast operation, which would even lead to the erroneous operation. Therefore, a low voltage sense amplifier with better performance is needed.

The Proposed Sense Amplifier

The proposed SA is shown in Figure 3. We can observe that there are only three transistor stages cascaded from VDD to GND. Note that the transistor stage number is less than that of CLSA, and the input nodes B, B are isolated to output nodes O, Ob. It is expected that the proposed SA has the same power consumption as CLSA, meanwhile a better performance at lower working voltage can be obtained. The circuit operation is described as follows. In Precharge Mode, the sensing signal SE is at logic 0. In this mode, the data on output nodes must be cleared and the SA prepares for next sensing operation. Because the sensing signals SE=0 and SE =1, MP1, MP4, MN5 and MN6 turn on, meanwhile MP5, MP6 turn off.

Thus the input signals from bit lines can't enter through MP5 and MP6. Nodes 1 and 2 are pulled down to GND level by MN5, MN6, so MN3, MN4 will be cut off. The precharge transistors MP1, MP4 charge the output nodes to VDD. Because MN3, MN4 are turned off, both the output nodes will hold at VDD level. In this time interval, the operation detail is shown in Figure 4(a).

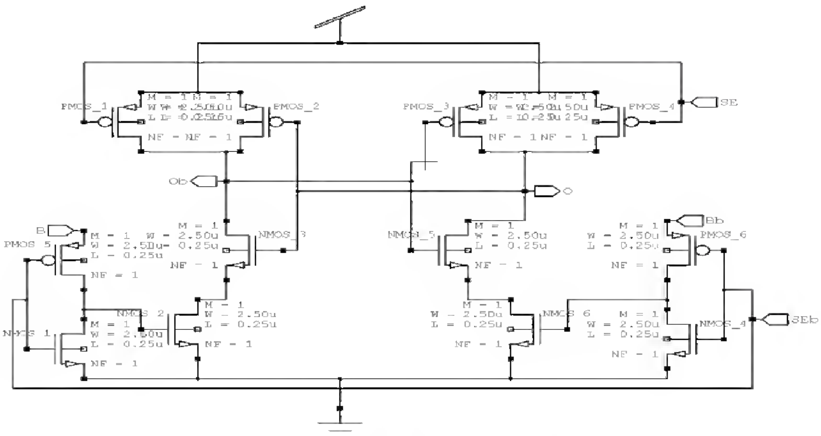
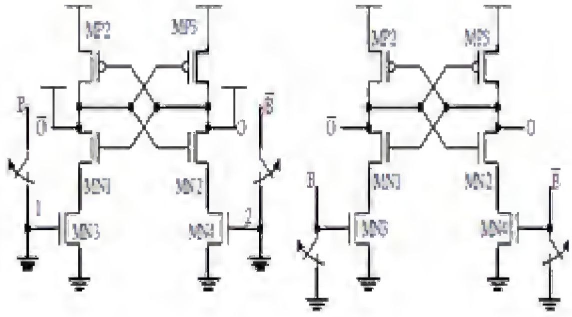


Figure 3: The Proposed Sense Amplifier

In Sense Mode, the sensing signal SE is at logic 1. In this mode, the bit line input signals, and B must be transferred to SA's differential input nodes 1 and 2. Therefore, MN3 and MN4 work as a common source differential amplifier. This operation situation is just like CLSA in sensing operation. As the sensing signals SE=1 and SE =0, MP5, MP6 turn on and MN5, MN6, MP1, MP4 turn off. The bit line signals are transferred to nodes 1 and 2 by MP5 and MP6.



(a) (b)

Figure 4: The Proposed SA Operation Diagrams (a) Precharge Mode (SE=0) (b) Sense Mode (SE=1)

The voltage difference between nodes 1 and 2 induces a drain-to-source current difference between MN3 and MN4. Finally, the cross-coupled amplifier constructed by MP2, MP3, MN1 and MN2 will convert and amplify the current difference to a voltage difference between output nodes O, and Ob. For a very short time, the full swing logic value appears on output nodes. This operation detail is shown in Figure 4(b). Thus, a modified CLSA with reduced transistor stage is achieved. The sensing speed and power consumption get better and we will show simulation results in the next section. But the area of the proposed SA is larger than that of CLSA.

Simulation Results and Comparison

Figure 5 shows the simulation waveform of the proposed SA based on TSMC 180nm CMOS process, and the working voltage is 1.2V. Two 1pF capacitances are loaded on both the bit lines respectively. Two SRAM cells with different storage data value are put on bit lines and used as the sources of input signal. The word line signal and sensing control signal are indicated by SE whose frequency is 100MHz. Under the simulation condition mentioned above, the simulation results are summarized in Table 1. In Table 1, H.S.D and F.S.D indicate the half and 90% of VDD sensing delay. PDP-H (Wsec) and PDP-F (Wsec) are the power delay product term of H.S.D and F.S.D. The half and 90% of VDD sensing delay are the time interval that begins at the beginning of rising edge of SE and ends wherein the output voltage difference of the SA are 50% and 90% of VDD, respectively. Both of two sensing delays shown in Table 1 have above improvement compared with CLSA. The power consumption of the proposed SA is 0.237 uW and it gets 59% improvement over CLSA.

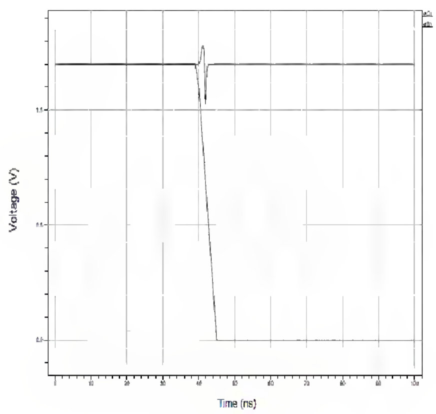


Figure 5: Simulation Waveform of the Proposed SA at 1.2 V

Table 1: Simulation Results and Comparison

	Proposed SA	CLSA	Conventional SA
Power	0.237 uW	0.18 uW	0.55 uW
HSD	3.1 ns	3.65 ns	3.1 ns

CONCLUSIONS

Simulation results and comparison shows that the proposed sense amplifier which is implemented in 180nm CMOS process can work at 100MHz with voltage as low as 1.2V. The improvement of sensing delay is reduced by 16% for various outputs loading. As the sense amplifier works at 1.2V, the simulations show that this design has 59% power improvement over the conventional sense amplifier.

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